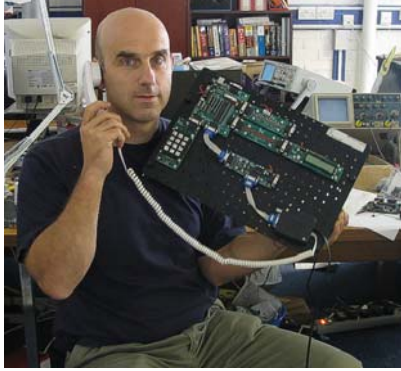


CPLD / FPGA programming and with E-blocks

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About this presentation



- This presentation was developed by John Dobson – Managing Director of Matrix Multimedia Limited.
- PowerPoint versions of this presentation are available on request.
- Notes on the presentation are included with each slide down here:

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Why study CPLD/FPGA programming?

- A modern context for Digital Electronics
- Death of the 74xxx device
- You can make complex circuits with ease
- A key skill that industry wants – particularly 'System on Chip' design

Some definitions

- CPLD: Complex Programmable Logic Device
- FPGA: Field Programmable Gate Array

These do essentially the same thing with different technologies...more later

What do they do?

- These are reprogrammable logic devices
- Designers use software to develop any digital circuit they like and the program the chip to perform the function
- They are very fast – much faster than a microcontroller

A modern CPLD

- The equivalent of 13 22V10s in one chip
- 128 flip flops or Logic Elements
- Electrically reprogrammable
- Can be programmed in a number of different languages
- \$10 (mid volume)

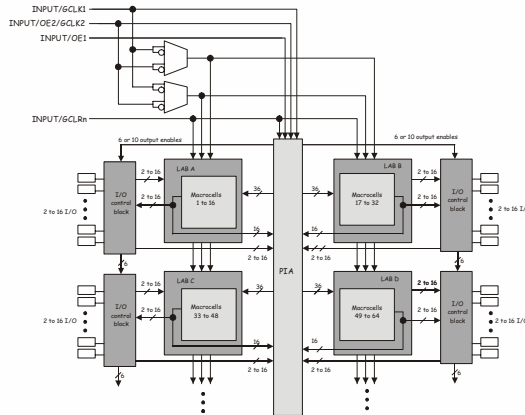


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Modern CPLDs effectively consist of a number of PLDs in the same package.
Electrically erasable now.

Modern CPLD architecture

- Not really important from a user's point of view – the software takes care of it.



An FPGA

- The equivalent of 400 22V10s in one chip
- 4000 flip flops (you can get them with 250,000)
- Electrically reprogrammable
- Can be programmed in a number of different languages
- \$15 (and falling)
- Only available in inconvenient surface mount packages



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FPGAs are optimised for production, not for education. This package is one of the smallest available. This is a 144 pin device. Pitch of leads is less than half a mm. Almost impossible to solder manually. Other packages include Ball Grid Arrays which need very specialist equipment to solder.

Differences between CPLDs and FPGAs

	CPLD	FPGA
Logic Elements	Up to 500	Up to 250,000
Operating voltage	5V	3.3V external, 1.5V internal
Cost	Start at \$10	Start at \$15
Packaging	Some leaded	All SMT
Program retention	Yes	No – load at power up

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FPGAs have a vastly bigger gate count, but actually don't cost a great deal more than a CPLD. FPGAs are all 3.3V to reduce power consumption. FPGAs are only available in SMT which is very inconvenient. FPGA's need reprogramming each time they are powered up by a slave processor or serial memory.

Problems

- CPLDs and FPGAs have SMD packages that are very hard to work with.
- Most projects can be done with a microcontroller
- E-blocks allows you to easily create systems incorporating micros and CPLDs / FPGAs – you just snap them together
- FPGAs are 3.3V

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The physical disadvantages of using FPGAs in practice makes the E-blocks solution very appealing.

How do you program CPLD/FPGAs?

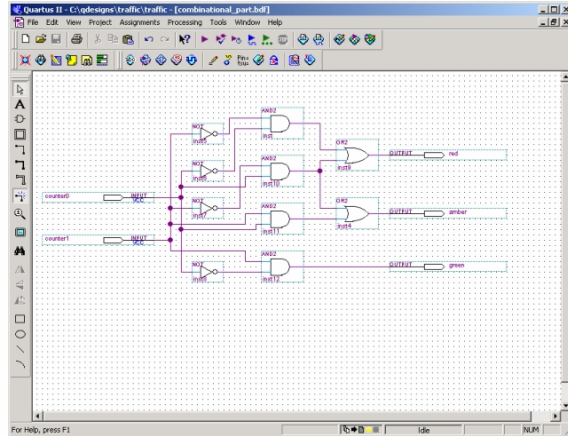
- Conventional logic symbols and circuits
- Descriptor languages
 - Verilog (prevalent in North America)
 - VHDL (prevalent in Europe)

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There is a wide choice here – people used to use DOS based applications like PALASM and WINCUPL. Network managers don't like these and support for them is dwindling as modern device manufacturers give away the design software. Verilog and VHDL are the choice of industry and this is the skill they want. It is convenient that you can also use conventional logic symbols in software packages.

Conventional symbols and circuits

- Develop a traditional schematic
- Compile
- Program the device



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Within Quartus II you can use conventional block diagrams to design your CPLD/FPGA.....

Descriptor languages

- More efficient way of describing logic behaviour
- A bit like C
- Most institutions migrate to a descriptor language

```
ENTITY decoder IS
PORT
(
  E3, N_E2, N_E1: IN bit;
  X: IN bit_vector(2 DOWNTO 0);
  Y: OUT bit_vector (7 DOWNTO 0)
);
END decoder;

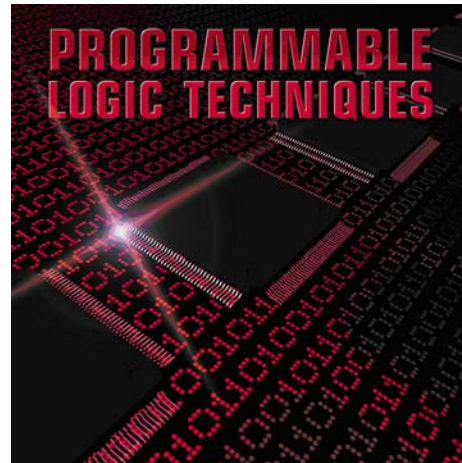
ARCHITECTURE behaviour OF decoder IS
--VHDL version of 74138
BEGIN
  PROCESS (E3, N_E2, N_E1, X)
  BEGIN
    IF (E3 AND NOT N_E2 AND NOT N_E1)='1'
    THEN
      CASE X IS
        WHEN "000" => Y <= "11111110";
        WHEN "001" => Y <= "11111101";
        WHEN "010" => Y <= "11111101";
        WHEN "011" => Y <= "11110111";
        WHEN "100" => Y <= "11101111";
        WHEN "101" => Y <= "11011111";
        WHEN "110" => Y <= "10111111";
        WHEN "111" => Y <= "01111111";
      END CASE ;
    ELSE
      Y <= "11111111";
    END IF ;
  END PROCESS ;
END behaviour;
```

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This will be unfamiliar to many. However if you look the language is close to English. If you look at the CASE statement you can see that the program decodes '111' to the 8 outputs all high. So with a little effort this is not too hard to understand

Programmable Logic Techniques

- Contains Quartus design software
- Course in VHDL (Europe)
- Course in Verilog (Americas)
- Currently free with CPLD solution

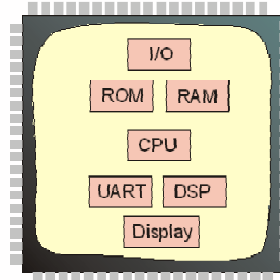


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Programmable Logic Techniques CD Rom contains a course in both VHDL and Verilog.

System on chip

- FPGA technology allows you to embed a processor, ROM, RAM, DSP, and any other block onto a single chip
- This is replacing a lot of Application Specific Integrated Circuit chips
- This has major advantages for electronics companies in terms of cost, reliability, reusability of intellectual property, and time to market



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System on Chip is a skill that is in great demand. This design methodology is becoming increasingly popular as FPGA costs fall.

A curious thing

- The skills and techniques for programming CPLDs are the same as those for programming FPGAs
- If you can program CPLDS, you can program FPGAs

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Whilst FPGA design is the skill industry wants, CPLD trainers can deliver the bulk of the course in many cases. FPGAs have significant advantages over CPLDs for learning when it comes to embedding microprocessors into designs – Universities and industry only at this stage – CPLD training solutions will be find for most vocational schools and colleges.

A key benefit of the E-blocks system

- E-blocks CPLD and FPGA boards are ready
- The FPGA board fits on top of the CPLD board (remove CPLD chip)
- The upgrade path is easy

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The expandability of the CPLD board to include FPGA design is a great benefit.

Part 3 – The E-blocks solutions

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CPLD solution

- A CPLD programmer and a few E-blocks
- Also a low cost PIC board so they can use the CPLD in conjunction with a microprocessor



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The low cost PIC board is included to allow students to create frames of reference for the CPLD – the CPLD board can do the fast stuff as a slave of the Microprocessor. For example it would be nice to get the CPLD to generate the TV signal framework, and to get the micro to generate the characters.

FPGA solution

- Includes a CPLD programmer and an FPGA programmer...
- ...as well as E-blocks boards which make the kit suitable for using with NIOS embedded microprocessor IP
- System On Chip ready

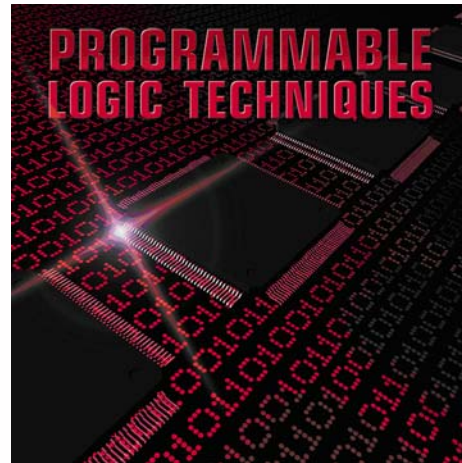


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Those that want FPGA equipment will probably only want it because they are interesting in combining embedded NIOS processors from Altera and combining with other circuitry on a single chip. The solutions we provide allow this to be done very easily. Note that the FPGA solution is relatively expensive. This is because it includes a lot of additional boards that facilitate the development of complete computer systems around this technology.

CPLD software solution

- CD ROM course with course in VHDL and Verilog programming
- CD ROM is supplied with each solution
- Uses Altera's Quartus II Web edition software (Free) which must be registered with Altera



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